High-Efficiency, Packaged Ka-Band MMIC Operating at 24 Volts

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Abstract

A power MMIC, employing a unique series bias scheme, is presented operating over the 31 to 33 GHz band. Mounted in a low cost metal-ceramic package and operating at 24 volts, this IC has demonstrated an output power of 0.81 watt with a power-added efficiency of 32%.

Introduction

While power MMIC technology has recently made great strides at Ka-band frequencies with power levels reaching 1 watt, the efficiency in general has been poor, typically less than 25% [1,2]. Further, the chip supply voltage for maximum efficiency is low, typically only 4 volts [1]. This low voltage causes problems for the user, further degrading the system efficiency due to excessive losses in the system power conditioning circuitry (DC-to-DC converter and series voltage regulator). In addition, package losses contribute to this system efficiency problem. The result, typically, is a system efficiency which degrades from a respectable chip efficiency of 25% to a dismal 15% or less at the system level.

It is the purpose of this paper to report a new high-voltage approach which addresses this voltage problem while achieving state-of-the-art performance in a low cost ceramic package.

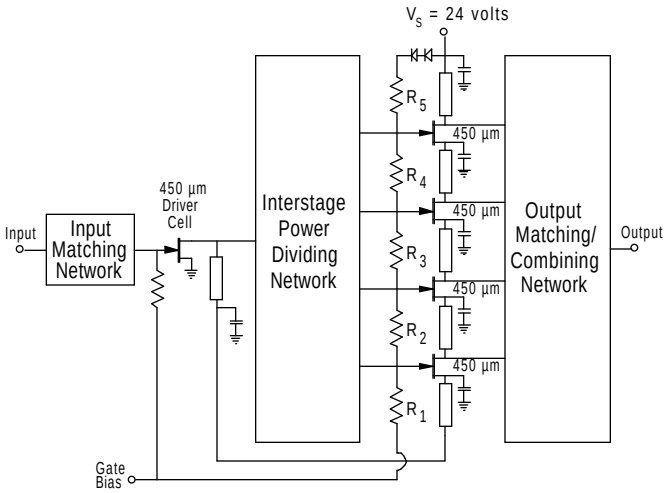

Figure 1. High Voltage, Series Bias Approach

The ICs reported in this paper were fabricated at TRW's GaAs IC foundry in Redondo Beach, CA. The PHEMT process and chip performance are described in [3] and [4], respectively.

Design Approach

The high voltage approach is shown conceptually in Figure 1. It consists of a 2-stage configuration with a single 450 µm cell driving four 450 µm cells. All 5 cells on the chip are biased in series instead of in parallel. This results in a chip supply voltage of 5 times the V_{DS} of an individual cell and a current level of 1/5 that of a similar IC employing conventional parallel biasing. The bias voltage for the individual cells is set by the resistive divider network, R_1 through R_5 in Figure 1. The resistors, nominally

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identical in value, produce equal voltage drops across each of the cells.

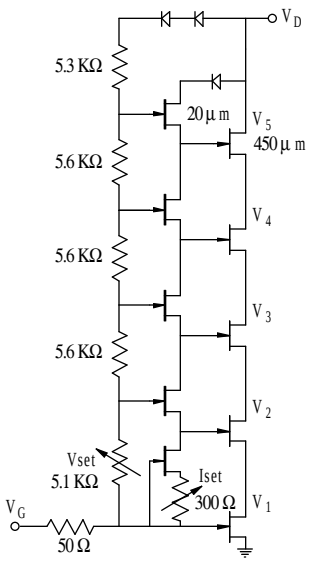

Figure 2. DC Equivalent Circuit of the Active Bias Network

While this passive bias scheme works in principle, if any one cell draws excessive gate current, it can disturb the voltage division in the resistive divider network, and over-voltage one or more cells in the array. We have devised a new active bias network, shown in Figure 2, which solves this problem. It incorporates a second string of series cells to act as a buffer between the resistive divider network and the RF cell array. This improves the stability of the voltage divider network by a factor of 10 or more. The gate periphery of the devices in this secondary string is only 20 µm per cell, and consequently, they do not dissipate a great deal of DC power. The entire bias network (resistors and active devices) requires a bias current of only 2 mA. This is less than 2% of the nominal chip bias current.

The measured voltage tracking, with supply voltage, is shown in Figure 3. Each cell receives almost exactly 1/5 of the supply voltage as it is varied from 0 to 20 volts.

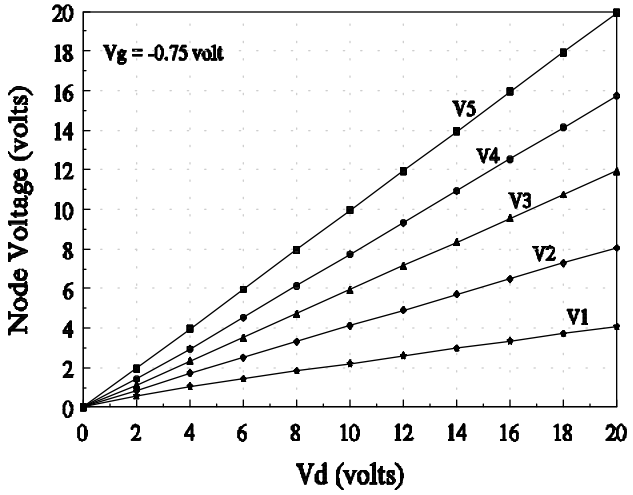

Figure 3. Voltage Tracking in the Active Bias Network

Packaging

The chips were mounted in a commercially available metal-ceramic package, model SEC-580237 from StratEdge. The package employs a copper-tungsten thermal base and a ceramic ring with 50 Ω and bias feedthrus. The cost of this package is less than $15 each in production

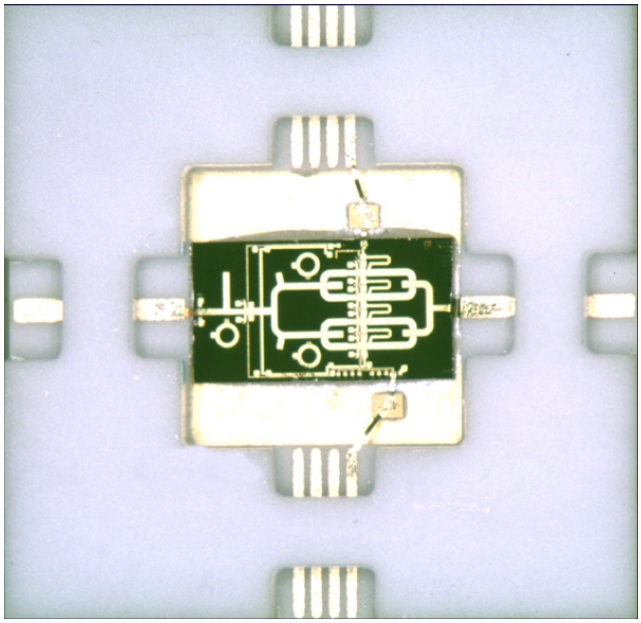

Figure 4. High-Voltage, Ka-band MMIC Mounted in a Metal-Ceramic Package

quantities. The chips were mounted with silver-loaded conductive epoxy and the RF and DC connections were completed with ribbon-bonds. A photograph of the chip mounted in the package is illustrated in Figure 4. The chip and package dimensions are 2 x 3.84 mm^2 and 8.9 x 8.9 mm^2 respectively. As shown, two 120 pF capacitors
(Dielectric Lab's di-caps) were mounted adjacent to the chip at the drain and gate bias pads for RF bypass and stability. In addition, two 0.1 µF capacitors (not shown) were connected to the fixture gate/drain bias terminals for low frequency (100 MHz and less) stability.

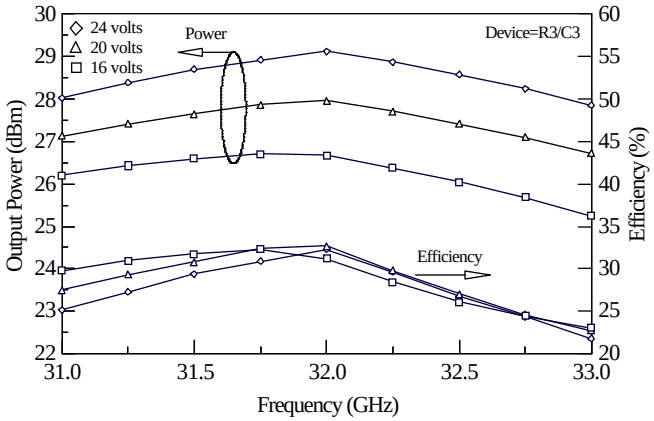

Figure 5. Power-Frequency Response of the Packaged Chip

Performance

Four chips were packaged and tested at Ka-band, and all of the chips performed similarly. The typical power performance, across the 31 to 33 GHz band, is illustrated in Figure 5. For these tests, the input power was fixed at 12 dBm. The results for three different bias voltages (16, 20 and 24 volts) are shown in this figure. These results indicate a passband centered at 32 GHz and a maximum output power of 29 dBm for V_D = 24 volts. For the lower bias voltages (16 and 20 volts), the power results are comparable to previous bare-chip results [4]. However, at higher voltages, 24 volts and above, the output power seems to saturate prematurely. Also, compared to the bare chip results, the center frequency is shifted lower in frequency by approximately 1 GHz and the bandwidth is reduced somewhat from 2.5 to 2 GHz. We believe that both effects are due to the parasitics of the package interacting with the chip input/output impedances. The results indicate that the output matching conditions may be closer to a power match at 20 volts than an efficiency match. This conclusion is further supported by the DC current level, which is too high for high-efficiency operation.

The package parasitics affect not only the bandwidth and output power, but they degrade the efficiency both directly through package dissipative losses and indirectly by reactive mismatch losses (non-optimum terminations). In spite of these parasitics, the maximum power-added efficiency ranged from 32 to 35 percent for all the packaged chips. While not as impressive as the previous bare-chip results (PAE as high as 41% [4]), these results are nonetheless notable.

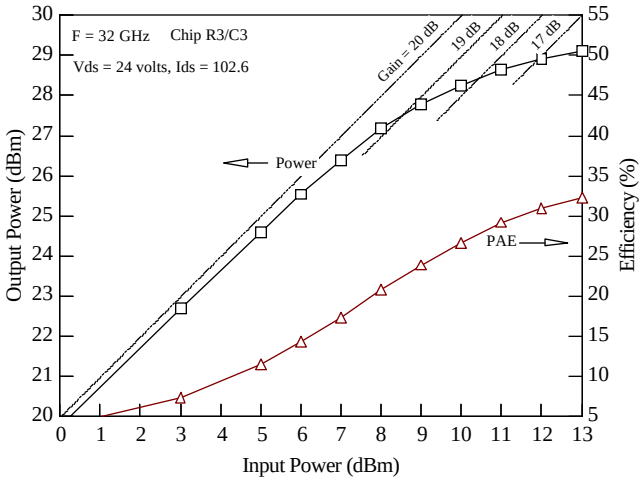

Figure 6. Output Power and Efficiency of the Packaged Chip at 32 GHz

The power transfer curve for a typical packaged chip, biased at 24 volts, is shown in Figure 6. The small signal gain is 19.5 dB, and the maximum output power is 29.1 dBm or 0.81

watt. The power-added efficiency is 32% at this point. As a "packaged" device, this is equal to or better than the best previously published "chip" result.

Conclusion

The above results represent new levels of performance for packaged MMICs operating at Ka-band frequencies. While comparable power levels have been reported, until now, no one has simultaneously achieved both high power (~1 watt) and good efficiencies (>30%) in a packaged IC. The efficiency results reported in this paper are at least 10 percentage points higher than the best previously reported packaged MMIC results at this frequency. Further, these results were achieved using a unique series bias scheme which results in a low current, high voltage chip bias.

Acknowledgment

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